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EXAMINER	
LE, JOHN H	

ART UNIT	PAPER NUMBER
2863	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/787,251	SLOTHERS ET AL.	
	Examiner	Art Unit	
	JOHN H. LE	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-61,63-66 and 68-80* is/are pending in the application.

4a) Of the above claim(s) *62 and 67* is/are withdrawn from consideration.

5)☒ Claim(s) *38-58,66,68,69,80 and 81* is/are allowed.

6)☒ Claim(s) *1-8,19-26,59-61,63-65 and 70-77* is/are rejected.

7)☒ Claim(s) *9-18, 27-37, 78-79* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Amendment

1. This office action is in response to applicant's amendment received on 10/12/2007.

Claims 1, 19, 59-61, 66, 69, 70, 73, 75, and 77 have been amended.

Claims 62 and 67 have been cancelled.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 19, 60, and 63 are rejected under 35 U.S.C. 102(b) s being anticipated by Back Ground Invention (BGI).

Regarding claims 19, 60, 63, BGI teaches a method of generating an output dependent upon the impedance or at least one component of the impedance of a device (sensor 1), the method comprising: connecting a load component (2) having a known impedance or at least one component thereof in series with said device (1)(BGI , Fig.1); applying a time-varying electrical signal to the series connected load component (2) and device (1)(e.g. BGI, Fig.1, page 2, lines 6-10); using a measurement channel to sequentially measure a first voltage (Vo) on a first side of said load component, and one of a second voltage (Vs) on a second side of said load component or a voltage difference across said load component (2)(BGI, Fig.1, page 2, lines 10-16) ; and (processor 3)

processing the sequentially measured voltages to generate an output dependent upon said impedance or at least one component of the impedance of said device (1)(BGI, Fig.1, page 2, lines 10-16, page 4).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 20-23, 25-26, 61, and 64-65 are rejected under 35 U.S.C. 103(a) as obvious over Back Ground Invention (BGI) in view of Slates et al. (US 2003/0222639).

Regarding claim 20, BGI fails to teach said signal is generated as a signal comprising sequential signal blocks for application to said series connected load component and device, wherein said measurement channel is used to measure each of said voltages during the same part of the signal block of sequential signal blocks of said signal.

Slates et al. teach said signal is generated as a signal comprising sequential signal blocks for application to said series connected load component and device (e.g. [0093]), wherein said measurement channel is used to measure each of said voltages during the same part of the signal block of sequential signal blocks of said signal (e.g. [0017]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to inform said signal is generated as a signal comprising sequential signal blocks for application to said series connected load component and device, wherein said measurement channel is used to measure each of said voltages during the same part of the signal block of sequential signal blocks of said signal as taught by Slates et al. in a method of generating an output dependent upon the impedance of BGI for the purpose of providing a unique digital system for digitally measuring an unknown electrical impedance (Slates et al., [0010]).

Regarding claim 21, Slates et al. teach storing a signal pattern for at least a part of a signal block, digitally generating a digital signal by repeatedly using the stored signal pattern (e.g. [0103]), and digital-to-analogue converting the digital signal to generate the signal (e.g. D/A converter 140, Fig.1).

Regarding claim 22, Slates et al. teach the signal generation and the processing are synchronous (e.g. [0278]).

Regarding claim 23, Slates et al. teach using a plurality of said measurement channels for measuring said voltages, using each of said measurement channels to sequentially measure said voltages to allow simultaneous measurements in the measurement channels, and processing the sequentially measured voltages for each channel (e.g. [0093]).

Regarding claim 25, Slates et al. teach processing generates the output as a measure of impedance or at least one component of the impedance of said device (e.g. [0191]).

Regarding claim 26, Slates et al. teach generate said output as an indication of whether or not a factor related to the impedance or at least one component thereof is above or below a threshold (e.g. [0257]).

Regarding claims 61, 64-65, BGI disclose an apparatus for generating an output dependant upon the impedance or at least one component of the impedance of a device (1)(Fig.1), the apparatus comprising: a load component (2) having a known impedance or at least one component thereof for connection in series with said device (1)(BGI , Fig.1); a generator (6) arrangement for application to the series connected load component (2) and device (1)(e.g. BGI, Fig.1, page 2, lines 6-10); a measurement arrangement (ACD1, LPF1, ACD2, LPF2) for measuring the voltage across said device (1) and a voltage across said load component (2) to obtain a measurement of the current in said device (1)(BGI, Fig.1, page 2, lines 10-16); a test load component (2) having a known impedance or at least one component thereof for connection place of said device (1) and in series with said load component (2)(BGI , Fig.1) and signal processing means (processor 3) for obtaining measurements indicative of a first voltage (Vo) on one side of said test load component, and a second voltage (Vs) on the other side of said load component and current in said test load component (2)(BGI, Fig.1, page 2, lines 10-16); processing said measurements when said device (1) is connected to generate an output in dependence upon the impedance or at least one component of the impedance of said device (1) using the stored value (BGI, Fig.1, page 2, lines 10-16, page 4).

BGI fails to a calibration of said load component and calibration processing means for processing the measurements when said test load component is connected in place of said device to determine and store a value dependent upon the impedance or at least one component of the impedance of the load component.

Slates et al. teach a calibration of said load component and calibration processing means (110) for processing the measurements when said test load component is connected in place of said device to determine and store a value dependent upon the impedance or at least one component of the impedance of the load component (e.g. [0103], [0125], [127]-[0128]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to inform a calibration of said load component and calibration processing means for processing the measurements when said test load component is connected in place of said device to determine and store a value dependent upon the impedance or at least one component of the impedance of the load component as taught by Slates et al. in a method of generating an output dependent upon the impedance of BGI for the purpose of providing a unique digital system for digitally measuring an unknown electrical impedance (Slates et al., [0010]).

6. Claims 1, 6, 24, 59, 70-72 are rejected under 35 U.S.C. 103(a) as obvious over Back Ground Invention (BGI) in view of Freeman et al. (USP 6,816,797).

Regarding claims 1 and 59, BGI disclose an apparatus for generating an output dependant upon the impedance or at least one component of the

impedance of a device (1)(Fig.1), the apparatus comprising: a load component (2) having a known impedance or at least one component thereof for connection in series with said device (1)(BGI , Fig.1); a signal generating (6) arrangement for generating a time-varying electrical signal for application to the series connected load component (2) and device (1)(e.g. BGI, Fig.1, page 2, lines 6-10); a measurement channel for measuring voltages (BGI, Fig.1, page 2, lines 10-16); a measurement channel (ACD1, LPF1, ACD2, LPF2) to sequentially measure a first voltage (Vo) on a first side of said load component, and one of a second voltage (Vs) on a second side of said load component or a voltage difference across said load component (2)(BGI, Fig.1, page 2, lines 10-16); and a processing (processor 3) arrangement connected to said measurement channel for processing the sequentially measured voltages to generate an output dependant upon said impedance or said at least one component of impedance of said device (1)(BGI, Fig.1, page 2, lines 10-16, page 4).

BGI fails to a switch arrangement connected to said measurement channel for switching the measurement channel.

Freeman et al. teach a switch (22) arrangement connected to said measurement channel for switching the measurement channel (e.g. Fig.3, Col.4, lines 1-4, Col.6, lines 39-50).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a switch arrangement connected to said measurement channel for switching the measurement channel as taught by Freeman et al. in a method of generating an output dependent upon the

impedance of BGI for the purpose of providing a system or apparatus for measuring fuel cell voltage and impedance (Freeman et al., Col.3, lines 36-38).

Regarding claims 6 and 24, Freeman et al. disclose wherein said processing arrangement comprises a digital processing arrangement, and said measurement channels include a common multiplexer (22) arrangement and a common analogue-to-digital converter (70, 75) (e.g. Fig.1, Col.6, lines 36-50).

Regarding claim 70, BGI disclose a proximity sensor (1) for sensing the proximity of a target (Fig.1): an electrical component for sensing the proximity of the target, said electrical component having electrical properties that vary with the proximity of the target; a impedance component having a known impedance and a first end connected to a first end of said electrical component; a signal generator (6) connected to a second end of said impedance component for generating an electrical signal for application to the impedance component and electrical component; an analogue-to-digital converter (ACD1, ACD2) for receiving an electrical signal and for generating a digital signal; and a processor (3) connected to the analogue-to-digital converter (ACD1, ACD2) for receiving a digital voltage signal and for generating a proximity signal (e.g. Fig.1, pages 2-4).

BGI fails to teach a switch connected to switch between said first end of said impedance component and a second end of said impedance component, wherein said processor is adapted to control said switch to switch to connect to said first and second ends of said impedance component sequentially.

Freeman et al. teach a switch (22) switch between said first end of said impedance component and a second end of said impedance component (e.g. Fig.1, Col.4, lines 1-4, Col.6, lines 39-50), wherein processor (CPU 20) is adapted to control said switch to switch to connect to said first and second ends of said impedance component sequentially (e.g. Fig.1, Col.7, lines 47-60).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a switch (22) and a processor (CPU 20) is adapted to control said switch as taught by Freeman et al. in a proximity sensor for sensing the proximity of a target of BGI for the purpose of providing a system or apparatus for measuring fuel cell voltage and impedance (Freeman et al., Col.3, lines 36-38).

Regarding claim 71-72, BGI teaches the electrical component comprise a capacitor, inductor, and a resistor (BGI, page 2).

7. Claims 2-5, 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Back Ground Invention (BGI) in view of Freeman et al. (USP 6,816,797) as applied to claim 1 above, and further in view of Slates et al. (US 2003/0222639).

Regarding claim 2, BGI fails to teach said signal is generated as a signal comprising sequential signal blocks for application to said series connected load component and device, wherein said measurement channel is used to measure each of said voltages during the same part of the signal block of sequential signal blocks of said signal.

Slates et al. teach said signal is generated as a signal comprising sequential signal blocks for application to said series connected load component and device (e.g. [0093]), wherein said measurement channel is used to measure each of said voltages during the same part of the signal block of sequential signal blocks of said signal (e.g. [0017]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to inform said signal is generated as a signal comprising sequential signal blocks for application to said series connected load component and device, wherein said measurement channel is used to measure each of said voltages during the same part of the signal block of sequential signal blocks of said signal as taught by Slates et al. in a method of generating an output dependent upon the impedance of BGI for the purpose of providing a unique digital system for digitally measuring an unknown electrical impedance (Slates et al., [0010]).

Regarding claim 3, Slates et al. teach storing a signal pattern for at least a part of a signal block, digitally generating a digital signal by repeatedly using the stored signal pattern (e.g. [0103]), and digital-to-analogue converting the digital signal to generate the signal (e.g. D/A converter 140, Fig.1).

Regarding claim 4, Slates et al. teach the signal generation and the processing are synchronous (e.g. [0278]).

Regarding claim 5, Slates et al. teach using a plurality of said measurement channels for measuring said voltages, using each of said measurement channels to sequentially measure said voltages to allow

simultaneous measurements in the measurement channels, and processing the sequentially measured voltages for each channel (e.g. [0093]).

Regarding claim 7, Slates et al. teach processing generates the output as a measure of impedance or at least one component of the impedance of said device (e.g. [0191]).

Regarding claim 8, Slates et al. teach generate said output as an indication of whether or not a factor related to the impedance or at least one component thereof is above or below a threshold (e.g. [0257]).

8. Claims 73-76 are rejected under 35 U.S.C. 103(a) as being unpatentable over Back Ground Invention (BGI) in view of Macbeth et al. (US 2003/0156367 A1).

Regarding claims 73, 75, BGI disclose an apparatus and method for generating an output dependant upon the impedance or at least one component of the impedance of a device (1)(Fig.1), the apparatus comprising: a load component (2) having a known impedance or at least one component thereof for connection in series with said device (1) to allow for the measurement of a voltage drop across the load component (2) (BGI , Fig.1); a generator (6) arrangement for applying a time-varying voltage across the series connected load component (2) and device (1)(e.g. BGI, Fig.1, page 2, lines 6-10); a measurement (ACD1, LPF1, ACD2, LPF2) arrangement adapted to sequentially measure a first voltage (Vo) one side of said load component, and a second voltage (Vs) on the other side of said load component or a difference voltage comprising the voltage difference across said load device(BGI, Fig.1, page 2,

lines 10-16); and a signal processing (processor 3) arrangement for processing the measurements to generate an output dependant upon said impedance of said device (1)(BGI, Fig.1, page 2, lines 10-16, page 4).

BGI fails to teach wherein said signal processing arrangement is adapted monitor said measurements to detect fault conditions in said device and to output a warning output if a fault condition is detected.

Macbeth et al. teach monitor said measurements to detect fault conditions in said device and to output a warning output if a fault condition is detected (e.g. [0028].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include monitor said measurements to detect fault conditions in said device and to output a warning output if a fault condition is detected as taught by Macbeth et al. in a method and apparatus of generating an output dependent upon the impedance or at least one component of the impedance of a device of Slates et al. for the purpose of providing an electrical protection device which protects an electrical power distribution system supplying voltage from a secondary winding of a transformer through an electrically conductive path to the protection device includes an impedance detector which measures the impedance of the path (Macbeth et al., Abstract).

Regarding claims 74, 76, Macbeth et al. teach detects a fault condition when at least one said measurement is outside a predetermined threshold or range (e.g. [0006]-[0008]).

9. Claim 77 is rejected under 35 U.S.C. 103(a) as being unpatentable over Back Ground Invention (BGI) in view of Ise et al. (USP 4,622,535).

Regarding claim 77, BGI disclose a method of identifying a device (1) having an impedance characteristic as a function of frequency (e.g. Fig.1, pages 2-3, the method comprising: applying at least two frequency signals to said device (1); obtaining measurements indicative of the voltage across said device (1) and the current flowing through said device at said frequencies; processing said measurements in a multiplicative and non divisional manner to determine if a first factor related to the impedance or part of the impedance of the device at a first frequency (e.g. Fig.1, pages 2-3).

BGI fails to teach a predefined inequality relationship with a second factor related to the impedance or part of the impedance of the device at a second frequency, and identifying the device in dependence upon the predefined inequality relationship.

Ise et al. teach a predefined inequality relationship with a second factor related to the impedance and identifying the device in dependence upon the predefined inequality relationship (e.g. Col.3, lines 28-61).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to inform a predefined inequality relationship with a second factor related to the impedance and identifying the device in dependence upon the predefined inequality relationship as taught by Ise et al. in a method of identifying a device of BGI for the purpose of providing a receiving circuit capable of transmitting data to a receiving station over transmission wiring in a data

transmission system irrespective of variations in load impedance characteristics (Ise et al., Col.1, lines 34-39).

Allowable Subject Matter

10. Claims 38-58, 66, 68-69, 80-81 are allowed.

11. Claims 9-18, 27-37, 78-79 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 9, none of the prior art of record teaches or suggests wherein said processing arrangement is adapted to: determine a first parameter indicative of the complex amplitude of the first voltage on a first side of said load component connected to said device, and a second parameter indicative of the complex amplitude of the difference between the first and second voltages or said voltage difference; multiply each of the first and second determined parameters by the complex conjugate of the second determined parameter to generate third and fourth parameters respectively; and compare said third and fourth parameters to generate said output, or compare one or more components or derivatives of the third parameter and one or more components or derivatives of said fourth parameter to generate said output. It is these limitations as they are claimed in the combination with other limitations of claim, which have not been

found, taught or suggested in the prior art of record, that make these claims allowable over the prior art.

Regarding claim 15, none of the prior art of record teaches or suggests wherein said signal generating arrangement is adapted to generate said electrical signal comprising a plurality of frequency components and said processing arrangement is adapted to determine a first parameter indicative of the complex amplitude of the first voltage on said first side of said load component for each said frequency, and a second parameter indicative of the complex amplitude of the difference between the first and second voltages or said voltage difference for each said frequency, to multiply each of the first and second determined parameters by the complex conjugate of the second determined parameter to generate third and fourth parameters respectively, and to compare said third and fourth parameters to generate said output, or compare one or more components or derivatives of the third and fourth parameters to generate said output. It is these limitations as they are claimed in the combination with other limitations of claim, which have not been found, taught or suggested in the prior art of record, that make these claims allowable over the prior art.

Regarding claim 27, none of the prior art of record teaches or suggests wherein said processing includes determining a first parameter indicative of the complex amplitude of the first voltage on a first side of said load device connected to said device, and a second parameter indicative of the complex amplitude of a difference between the first and second voltages or said voltage

difference; multiplying each of the first and second determined parameters by the complex conjugate of the second determined parameter to generate third and fourth parameters respectively; and comparing said third and fourth parameters to generate said result. It is these limitations as they are claimed in the combination with other limitations of claim, which have not been found, taught or suggested in the prior art of record, that make these claims allowable over the prior art.

Regarding claim 33, none of the prior art of record teaches or suggests wherein said electrical signal comprises a plurality of frequency components and said processing includes determining a first parameter indicative of the complex amplitude of the first voltage on said first side of said load component for each said frequency, and a second parameter indicative of the complex amplitude of the difference between the first and second voltages or said voltage difference for each said frequency, multiplying each of the first and second determined parameters by the complex conjugate of the second determined parameter to generate third and fourth parameters respectively, and comparing said third and fourth parameters to generate said output, or comparing one or more components or derivatives of the third and fourth parameters to generate said output. It is these limitations as they are claimed in the combination with other limitations of claim, which have not been found, taught or suggested in the prior art of record, that make these claims allowable over the prior art.

Regarding claim 38, none of the prior art of record teaches or suggests wherein said processing arrangement is adapted to: determine a first parameter

indicative of the complex amplitude of the first voltage on a first side of said load component connected to said device, and a second parameter indicative of the complex amplitude of said difference voltage or a calculated difference voltage comprising the difference between the first and second voltages; multiply each of the first and second determined parameters by the complex conjugate of the second determined parameter to generate third and fourth parameters respectively; and compare said third and fourth parameters to generate an output or compare one or more components or derivatives of the third parameter and said fourth parameter to generate said output. It is these limitations as they are claimed in the combination with other limitations of claim, which have not been found, taught or suggested in the prior art of record, that make these claims allowable over the prior art.

Regarding claim 48, none of the prior art of record teaches or suggests wherein said processing comprises: determining a first parameter indicative of the complex amplitude of the first voltage on a first side of said load component connected to said device, and a second parameter indicative of the complex amplitude of said difference voltage or a calculated difference voltage comprising the difference between the first and second voltages; multiplying each of the first and second determined parameters by the complex conjugate of the second determined parameter to generate third arid fourth parameters respectively; and comparing said third and fourth parameters to generate said output or comparing one or more components or derivatives of the third parameter and said fourth parameter. It is these limitations as they are claimed in the combination with

other limitations of claim, which have not been found, taught or suggested in the prior art of record, that make these claims allowable over the prior art.

Regarding claim 66, none of the prior art of record teaches or suggests wherein said processing comprises: determining third and fourth parameters indicative of the complex amplitude, at said fist and second frequency respectively, of said of said difference voltage or a calculated difference voltage comprising the difference between the first and second voltages; multiplying each of the first and third determined parameters by the complex conjugate of the third determined parameter to generate fifth and sixth parameters respectively; multiplying each of the second and fourth determined parameters by the complex conjugate of the fourth determined parameter to generate seventh and eighth parameters respectively; and performing a comparison using said fifth, sixth, seventh and eighth parameters to determine said value; using said value to identify said device . It is these limitations as they are claimed in the combination with other limitations of claim, which have not been found, taught or suggested in the prior art of record, that make these claims allowable over the prior art.

Regarding claim 69, none of the prior art of record teaches or suggests wherein said processing comprises: obtaining third and fourth parameters indicative of the complex amplitude, at said fist and second frequency respectively, of said of said difference voltage or a calculated difference voltage comprising the difference between the first and second voltages; multiplying each of the first and third determined parameters by the complex conjugate of the third determined parameter to generate fifth and sixth parameters respectively;

multiplying each of the second and fourth determined parameters by the complex conjugate of the fourth determined parameter to generate seventh and eighth parameters respectively; and comparing at least one of parameters for said device with corresponding at least one parameters for at least one other device to identify said device . It is these limitations as they are claimed in the combination with other limitations of claim, which have not been found, taught or suggested in the prior art of record, that make these claims allowable over the prior art.

Regarding claim 78, none of the prior art of record teaches or suggests wherein said predefined inequality relationship defines whether said first factor is greater than or less than said second factor times a predetermined constant, said constant being predetermined for identification of the device. It is these limitations as they are claimed in the combination with other limitations of claim, which have not been found, taught or suggested in the prior art of record, that make these claims allowable over the prior art.

Regarding claim 79, none of the prior art of record teaches or suggests wherein said first frequency is below a frequency at which eddy current are small in the device. It is these limitations as they are claimed in the combination with other limitations of claim, which have not been found, taught or suggested in the prior art of record, that make these claims allowable over the prior art.

Response to Arguments

12. Applicant's arguments filed have been fully considered but they are not persuasive.

-Applicant argues that the prior did not teach “a switch arrangement connected to said measurement channel for switching the measurement channel to sequentially measure a first voltage on a first side of said load component, and one of a second voltage on a second side of said load component or a voltage difference across said load component” as cited in claims 1 and 59.

Examiner position is that Freeman et al. teach a switch (22) arrangement connected to said measurement channel for switching the measurement channel (e.g. Fig.3, Col.4, lines 1-4, Col.6, lines 39-50).

Examiner position is that BGI teach the measurement channel to sequentially measure a first voltage (Vo) on a first side of said load component, and one of a second voltage (Vs) on a second side of said load component or a voltage difference across said load component (2)(BGI, Fig.1, page 2, lines 10-16).

-Applicant argues that the prior did not teach “a measurement channel to sequentially measure a first voltage on a first side of said load component, and one of a second voltage on a second side of said load component or a voltage difference across said load component” as cited in claims 19 and 60.

Examiner position is that BGI teaches a measurement channel to sequentially measure a first voltage (Vo) on a first side of said load component, and one of a second voltage (Vs) on a second side of said load component or a

voltage difference across said load component (2)(BGI, Fig.1, page 2, lines 10-16).

-Applicant argues that the prior did not teach, "obtaining measurements indicative of a first voltage on one side of said test load component, and a second voltage on the other side of said load component and current in said test load component" as cited in claim 61.

Examiner position is that BGI teaches obtaining measurements indicative of a first voltage (Vo) on one side of said test load component, and a second voltage (Vs) on the other side of said load component and current in said test load component (2)(BGI, Fig.1, page 2, lines 10-16).

-Applicant argues that the prior did not teach, "a measurement arrangement adapted to sequentially measure a first voltage one side of said load component, and a second voltage on the other side of said load component or a difference voltage comprising the voltage difference across said load device" as cited in claims 73 and 75.

Examiner position is that BGI teaches a measurement (ACD1, LPF1, ACD2, LPF2) arrangement adapted to sequentially measure a first voltage (Vo) one side of said load component, and a second voltage (Vs) on the other side of said load component or a difference voltage comprising the voltage difference across said load device(BGI, Fig.1, page 2, lines 10-16)

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**.

See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CF 136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

14. Specifically Back Ground Invention (BGI), Ise et al., and Freeman et al. has been added to the other ground of rejection.

Contact Information

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHN H. LE whose telephone number is (571)272-2275. The examiner can normally be reached on 9:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John E. Barlow can be reached on 571 272 2269. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

John H. Le	/John E Barlow Jr./
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